REMARKS

In view of the above amendments and the following remarks, reconsideration of the objections and rejections is respectfully requested.

The specification and abstract have been reviewed and revised to improve their English grammar and U.S. form as well as address the new title requirement identified section 2 of the Office Action. The amendments to the specification and abstract have been incorporated into a substitute specification and abstract. Attached are two versions of the substitute specification, a marked-up version showing the revisions, as well as a clean version. No new matter has been added.

In accordance with the Examiner's request, the invention is now titled "DATA PROCESSING SYSTEM CONTAINING MULTIPLE DEDICATED PROCESSING UNITS CONNECTED VIA DATA TRANSFER UNITS TO A PROGRAM CONTROLLED CENTRAL PROCESSOR."

Claims 1-15 have been canceled without prejudice or disclaimer to the subject matter contained therein and replaced by new claims 16-20.

Original claims 7-9 were objected to by the Examiner. However, claims 7-9 have been canceled and replaced by new claims. Thus, the formal objections are considered moot based on the cancellation of claims 7-9.

Original claim 13 was rejected under 35 U.S.C. §112, second paragraph, on the basis of having insufficient antecedent basis. However, this rejection is considered moot based on the cancellation of original claim 13 because new claims 16-20 have been drafted specifically to avoid the problems identified by the Examiner and to otherwise clearly comply with 35 U.S.C. §112, second paragraph.

Claims 1-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sihlbom et al. (U.S. 6,653,859) in view of Zak et al. (U.S. 5,265,207). This rejection is clearly inapplicable to the new claims for the following reasons.

New Claims 16-20 are Patentable Over Sihlbom

New independent claim 16 recites a data processing system comprising in part, (1) a first data processing unit operable to perform data processing according to a program control; (2) a

plurality of second data processing units operable to perform data processing under wired logic control, and each of the plurality of second data processing units includes (a) a calculating unit; and (b) a selector unit; (3) a storage unit operable to store data; (4) a first data transfer unit operable to connect the first data processing unit with each of the plurality of second data processing units via the storage unit; and (5) a second data transfer unit operable to connect each of the plurality of second data processing units to each other, wherein (a) the second data transfer unit is operable to connect at least one of the plurality of second data processing units in series to another second data processing unit, and (b) the selector unit is operable to determine a destination of a data transfer from among each of the plurality of second data processing units, according to a link map table.

In contrast to the present invention as recited in new independent claim 16, Sihlbom teaches a heterogenous integrated circuit with reconfigurable logic cores. In particular, Sihlbom teaches an integrated circuit having a digital signal processor (DSP) and programmable logic cores (PLCs). The PLCs are coupled to the DSP through a DMA sharing unit. The DSP controls the PLC operations and can reconfigure one PLC while another PLC is processing data (see Abstract). Further, there is a common interface bus which couples the DSP with the PLCs (see col. 1, line 60-62). Sihlbom also teaches that a dedicated sharing unit (DSU) is used to provide data transfer between the DSP and the PLCs (see col. 6, lines 27-35; Fig. 9). Moreover, the DSU includes a scheduler which controls the switching of data ports within the DSU so that each port can transfer data for part of the bandwidth of the DSP (see col. 6, lines 61-66; Fig. 6). Further, the PLCs are arranged such that two PLCs receive data according to the scheduler within the DSU (see Fig. 9, elements 130, 141, 142 and 146).

Based on the above discussion, Sihlbom teaches PLCs which can be programmed and reconfigured according to instructions from a DSP. However, Sihlbom does not disclose or suggest a plurality of second data processing units operable to perform data processing *under wired logic control*. Simply stated, Sihlbom teaches programmable and reconfigurable processors but does not disclose or suggest second data processing units which process *under wired logic control*.

Moreover, Sihlbom teaches that a DSU that includes a scheduler which alternates the flow of data between two PLCs. However, Sihlbom does not disclose or suggest a second data transfer

unit operable to connect each of the plurality of second data processing units to each other, wherein at least one of the plurality of second data processing units is connected in series to another second data processing unit and wherein a selector unit within the second data processing unit is operable to determine a destination of a data transfer from among each of the plurality of second data processing units according to a link map table.

Accordingly, because Sihlbom does not disclose or suggest the *selector unit*, or the *wired logic control*, it is submitted that the Sihlbom reference does not anticipate or render obvious the invention as recited in new independent claim 16. Accordingly, it is respectfully submitted that new independent claim 16 and the claims that depend therefrom are clearly patentable over Sihlbom.

New Claims 16-20 are Patentable Over Sihlbom in View of Zak

In contrast to the present invention as recited in new claim 16, Zak teaches a parallel computing system including arrangement for transferring messages from a source processor to selected ones of a plurality of destination processors and combining responses. Specifically, Zak teaches processing elements (0-N) being connected in parallel (i.e., processing elements being arranged such that each processing element can transfer data to another processing element) (see Fig. 1, elements 11 and 14) and teaches processing units (LEAF 0-N) (see Fig. 2a, element 21) being arranged in parallel within parallel DR node groups (see Fig. 2a, element 20), but does not disclose or suggest at least one of said plurality of second data processing units being connected in series to another second data processing unit. Moreover, the Zak reference does not disclose or suggest the selector unit or the wired logic control as recited in new claim 16.

Accordingly, the combination of Sihlbom in view of Zak fails to disclose or suggest the features of new claim 16. Thus, it is apparent that new claim 16 and the claims that depend therefrom are patentable over Sihlbom in view of Zak.

Because of the above-mentioned distinctions, it is clear that new claims 16-20 are not anticipated by the Sihlbom or Zak references and are patentable over the references relied upon in the rejections. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of the invention would not have been motivated to combine the references or to make any combination of the references of record in such a manner as to

result in, or otherwise render obvious, the present invention as recited in new claims 16-20. Therefore, it is submitted that new claims 16-20 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance, and early notification thereof is earnestly requested.

Moreover, it is respectfully requested that the Examiner consider the foreign patent office application (CN 1302028) enclosed with the Information Disclosure Statement (IDS) filed on April 26, 2006. A copy of the IDS is enclosed herewith.

The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

Takashi HASHIMOTO et al.

By: _____

Nils E. Pedersen
Registration No. 33,145
Attorney for Applicants

NEP(ALD)/mjw
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
November 17, 2006